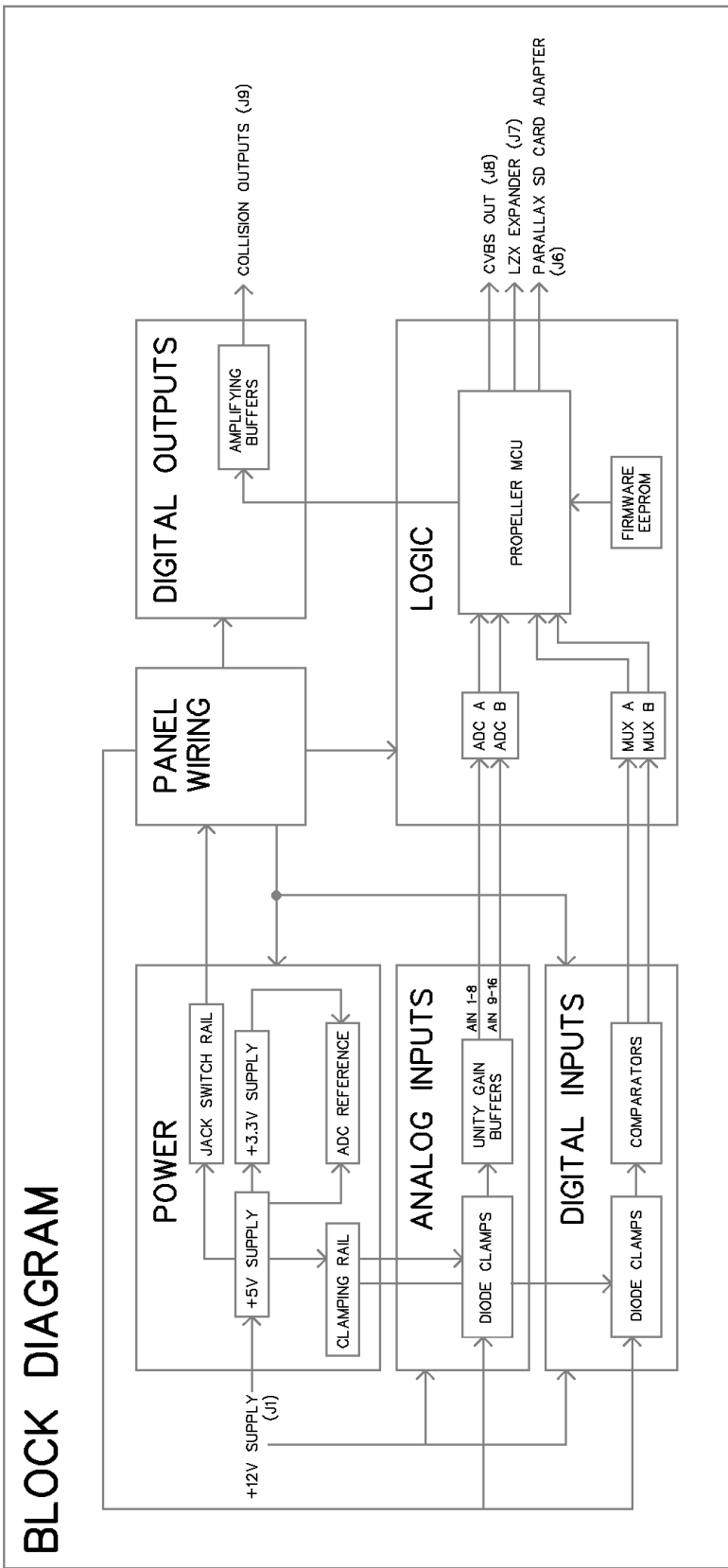
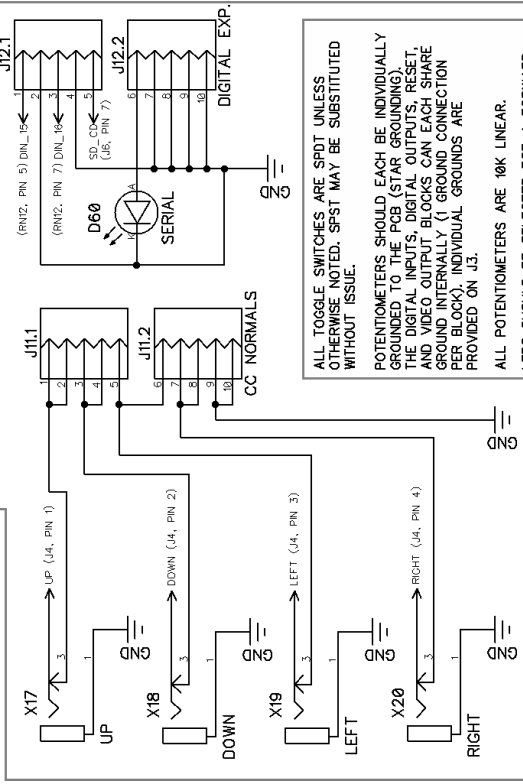


# MING MECCA WORLD CORE

DESIGNED BY JORDAN BARTEE IN PROVIDENCE, RI, WINTER 2013



# PANEL WIRING



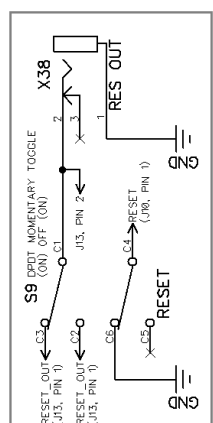
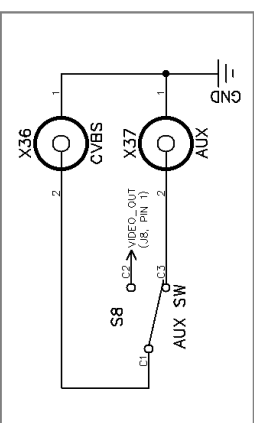
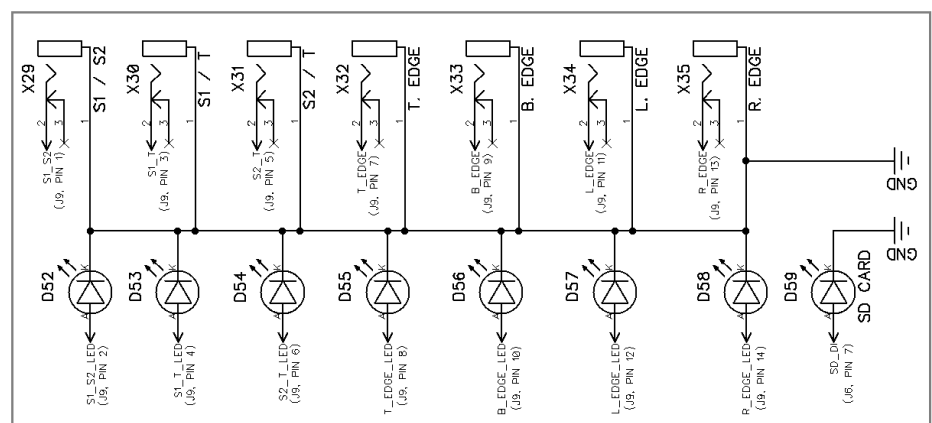
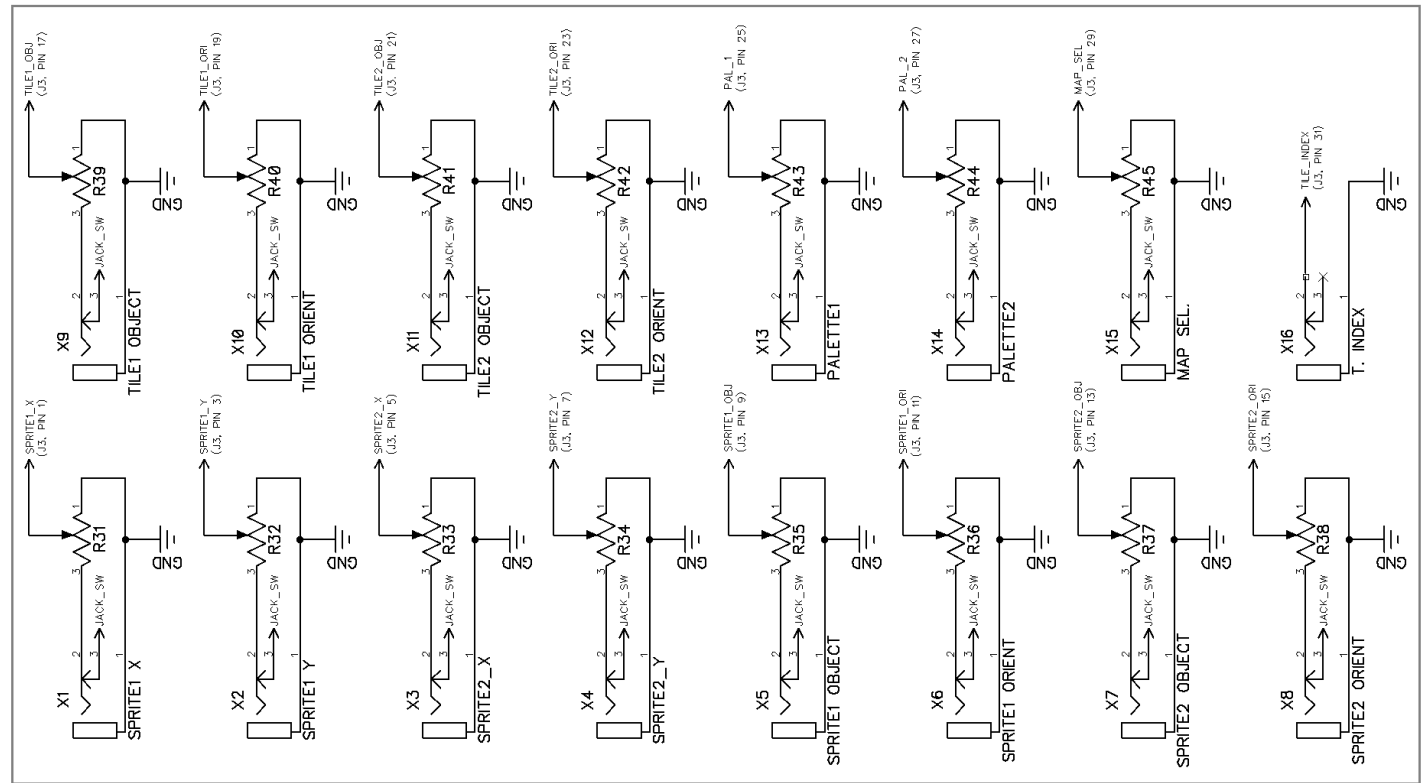
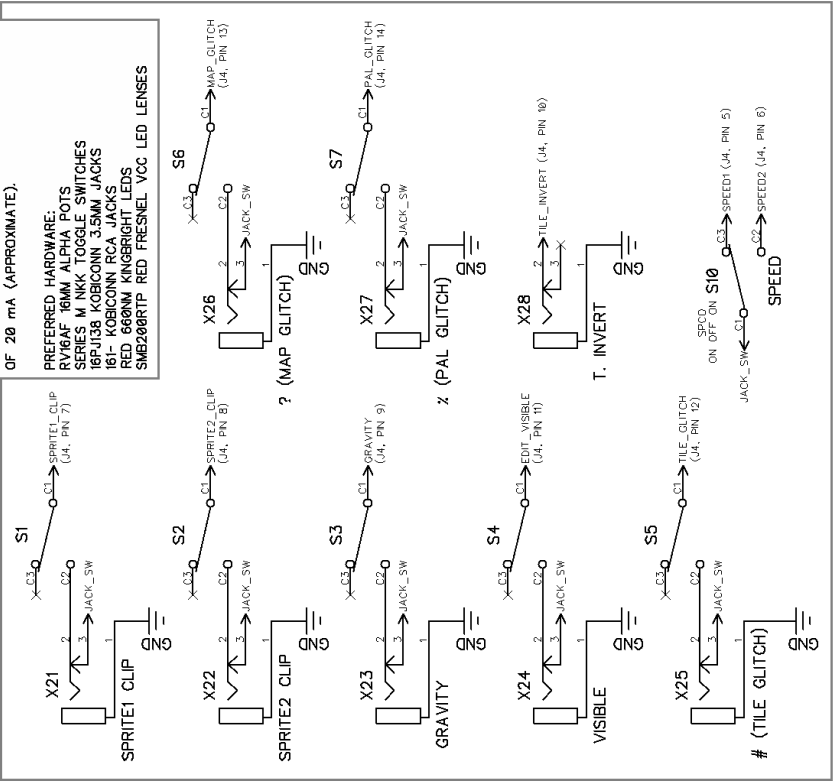
ALL TOGGLE SWITCHES ARE SPDT UNLESS OTHERWISE NOTED. SPST MAY BE SUBSTITUTED WITHOUT ISSUE.

POTENTIOMETERS SHOULD EACH BE INDIVIDUALLY GROUNDED TO THE PCB (STAR GROUNDING). THE DIGITAL INPUT BLOCKS CAN EACH SHARE AND VIDEO OUTPUT BLOCKS CAN EACH SHARE GROUND INTERNALLY (1 GROUND CONNECTION PER BLOCK). INDIVIDUAL GROUNDS ARE PROVIDED ON J3.

ALL POTENTIOMETERS ARE 10K LINEAR.

LEDS SHOULD BE SELECTED FOR A FORWARD VOLTAGE OF 2.5V AND A FORWARD CURRENT OF 20 mA (APPROXIMATE).

PREFERRED HARDWARE:  
 RY616AF 16MM ALPHA POTS  
 SERIES M NKK TOGGLE SWITCHES  
 I6PJ138 KOBICONN 3.5MM JACKS  
 I61- KOBICONN ROA JACKS  
 RED 660NM KINGBRIGHT LEDS  
 SMB208R1P RED FRESNEL VCC LED LENSES



# POWER

THE 7805 AND 7833 REGULATORS SHOULD BE HEATSUNK AND RATED FOR AT LEAST 280 mA EACH.

ALL CAPACITORS ARE CERAMIC EXCEPT WHERE NOTED.

IN ADDITION TO THE MAIN PSU SCHEMATICS ARE ALSO SHOWN FOR THE OP AMP AND COMPARETOR SUPPLIES. ADC REFERENCE, JACK SWITCH RAIL AND PROTECTION DIODE CLAMPING RAIL THE ABSOLUTE MINIMUM DECOUPLING CONFIGURATION IS SHOWN, CONSISTING OF A SINGLE 100nF CERAMIC CAPACITOR PER IC AND A 6.8uF TANTALUM CAPACITOR PER IC BLOCK. ALL ICs IN EACH BLOCK SHOULD BE GROUPED CLOSELY TOGETHER SINCE THEY SHARE THE TANTALUM CAPACITOR. ADDITIONAL DECOUPLING MAY BE NECESSARY DEPENDING ON PCB DESIGN.

GROUND PINS 5 AND 6 ON POWER CONNECTOR J1 ARE INTENTIONALLY LEFT UNCONNECTED TO PREVENT DAMAGING SHORTS FROM OCCURRING IF J1 IS CONNECTED BACKWARDS DUE TO USER ERROR. PINS 1, 2, AND 13 - 15 ARE ALSO LEFT UNCONNECTED.

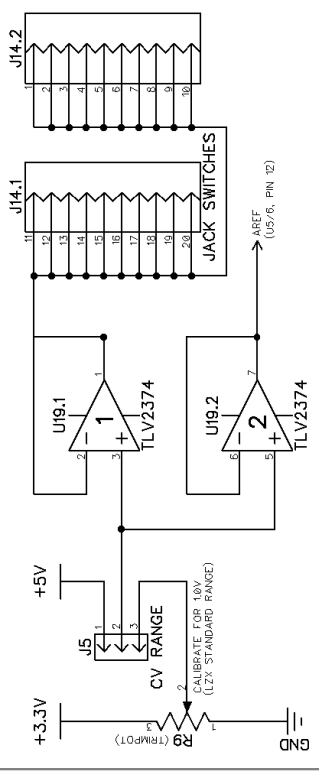
**12V SUPPLY**  
MULTIPLEXERS U7, U8  
COMPARATORS U9 - U12  
OP AMPS U13 - U19

**5V SUPPLY**  
ADCS U5, U6

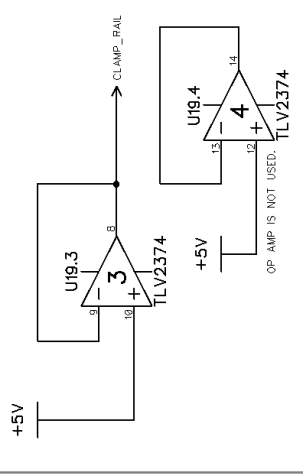
**3.3V SUPPLY**  
PROPELLER U3  
EEPROM U4  
SD CARD ADAPTER

**TOTAL CURRENT CONSUMPTION**  
APPROX. 216 mA

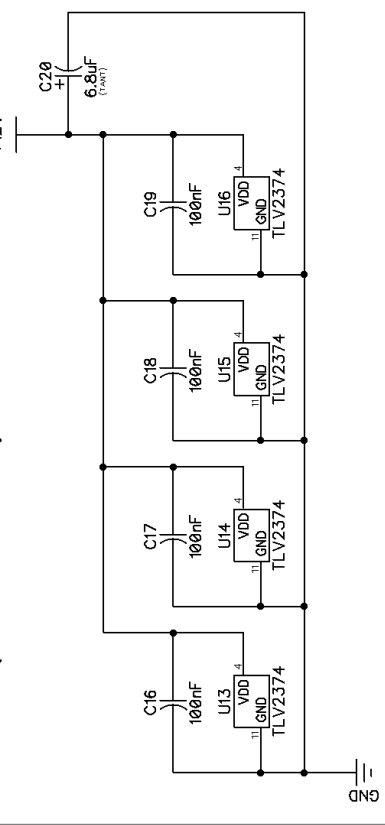
## ADC REFERENCE, JACK SWITCH RAIL



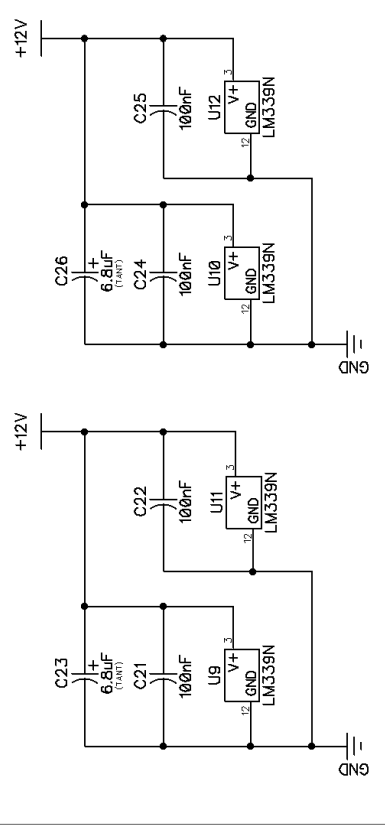
## CLAMPING RAIL



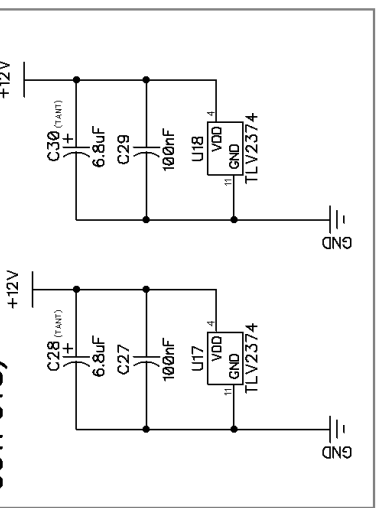
## OP AMPS (ANALOG INPUTS)



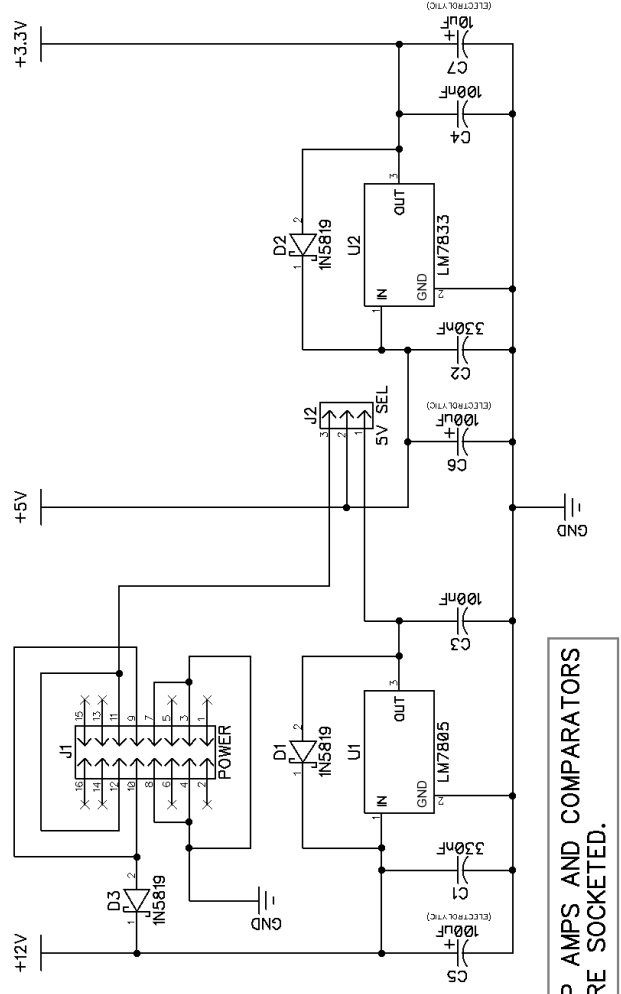
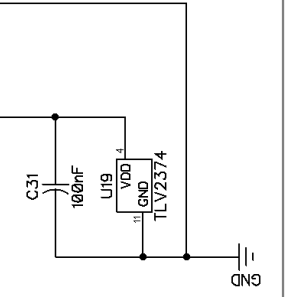
## COMPARATORS (DIGITAL INPUTS)



## OP AMPS (DIGITAL OUTPUTS)

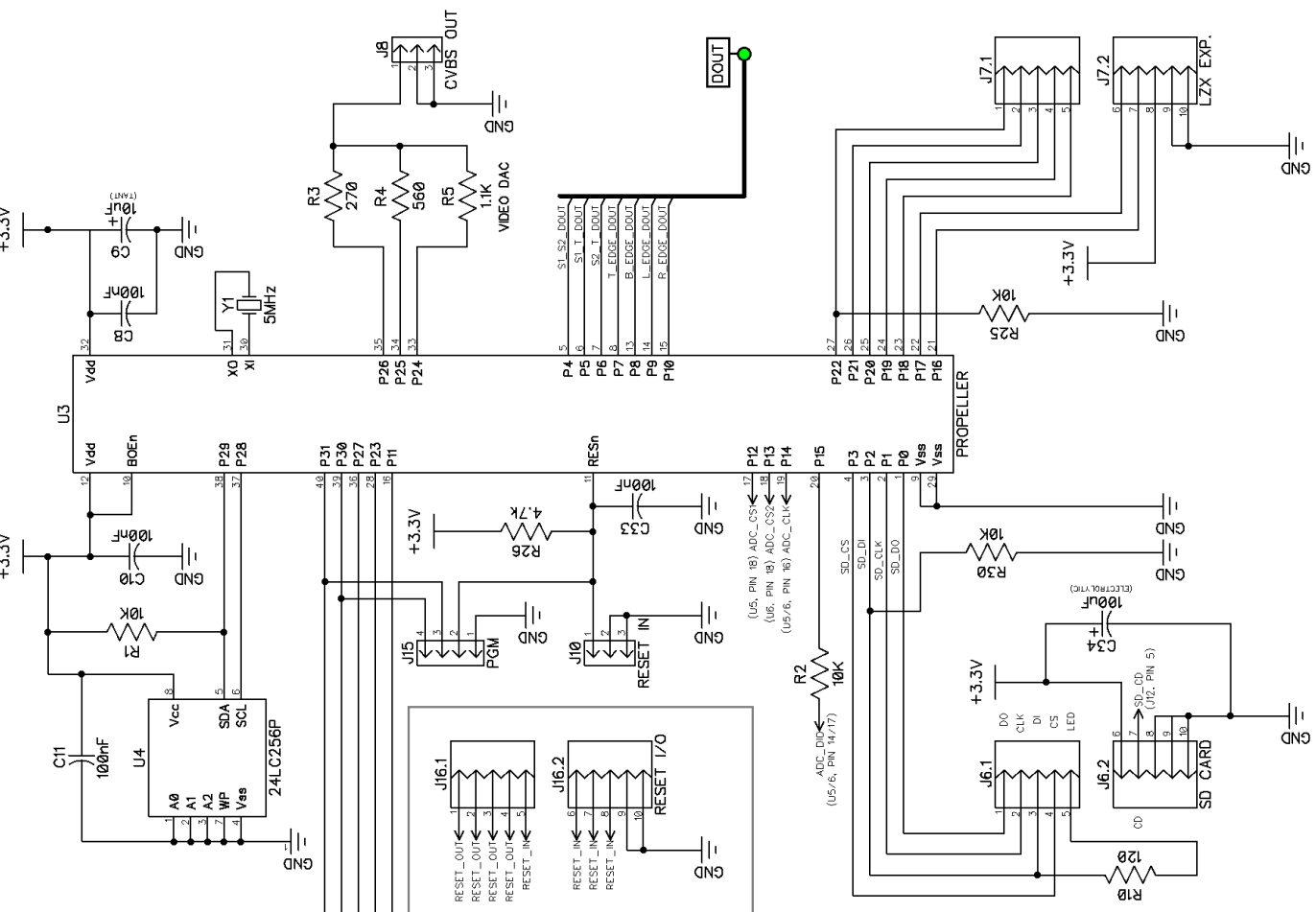
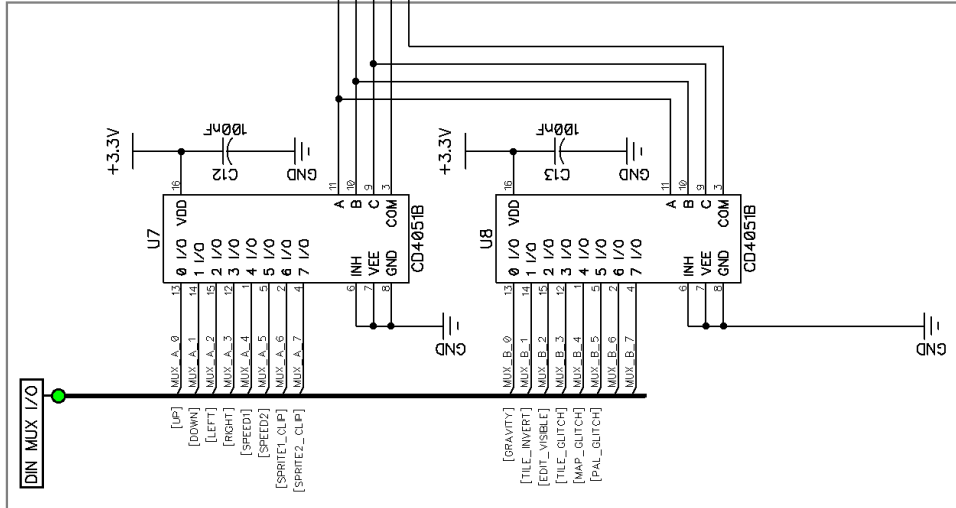
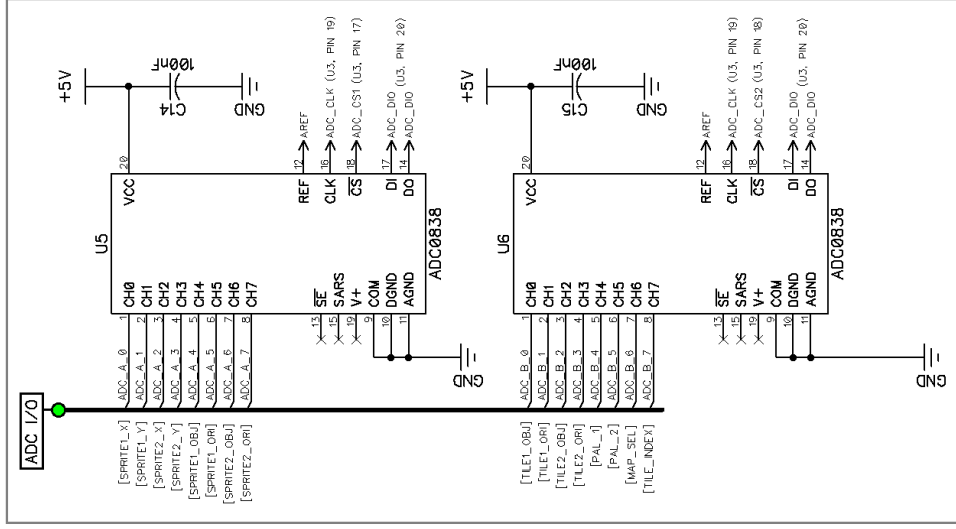


## OP AMPS (REF, SWITCH, CLAMP RAILS)



OP AMPS AND COMPARATORS ARE SOCKETED.

# LOGIC



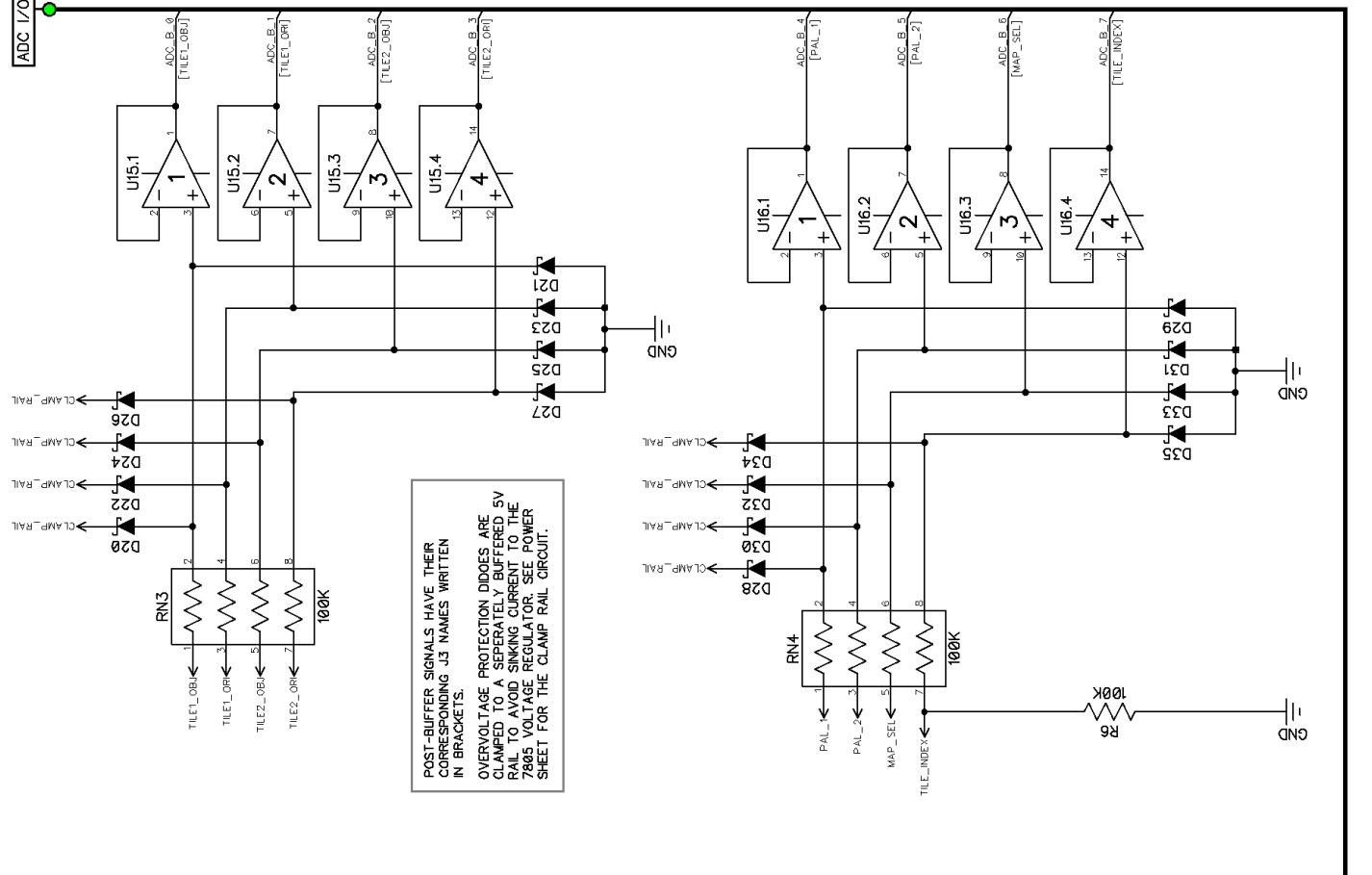
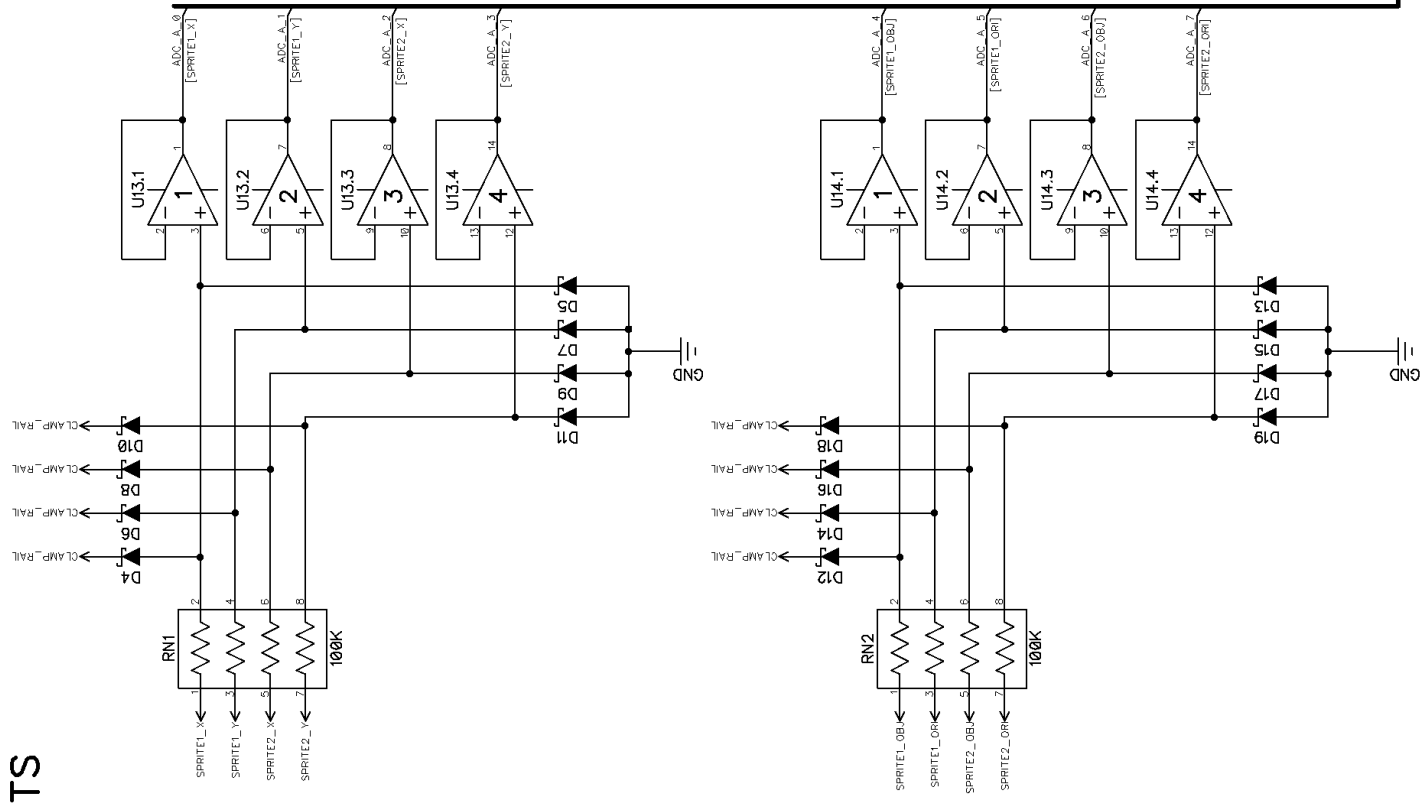
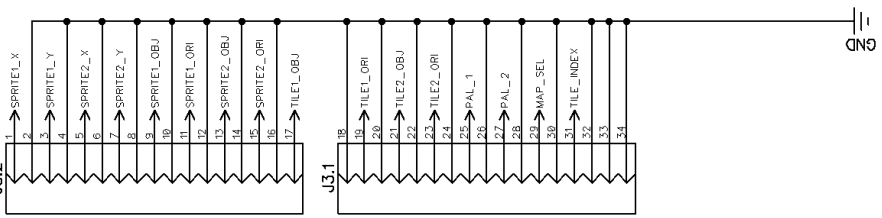
ALL RESISTORS ARE 5% TOLERANCE EXCEPT FOR R3 - R5, WHICH ARE 1% OR BETTER.  
 ALL CAPACITORS ARE CERAMIC EXCEPT WHERE NOTED.  
 ADC AND MUX I/O BUS SIGNALS HAVE THEIR CORRESPONDING J3 AND J4 NAMES WRITTEN IN BRACKETS.  
 THE PROPELLER'S RESn INPUT IS EXTREMELY SENSITIVE TO FLUCTUATIONS ON VSS AS WELL AS STRAY EMI. IN ADDITION TO THE CERAMIC DECOUPLING CAPACITOR C32, RESn IS TIED TO EXTERNAL PULL-UP RESISTOR R28. DEPENDING ON THE PCB DESIGN AND OPERATING ENVIRONMENT, R28 MAY NEED TO BE STIFFER, 2.2K OR 'K' ARE VALID SUBSTITUTIONS IF SPORADIC RESETS OCCUR.  
 THE PROPELLER PLUG-HEADER J15 SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE PROPELLER'S RESn INPUT (PIN 11) IN ORDER TO REDUCE LOADING AND INTERFERENCE.  
 THE 100nF ELECTROLYTIC CAPACITOR ACROSS J6'S SUPPLY STABILIZES POWER WHEN INSERTING OR REMOVING AN SD CARD. IT SHOULD BE PLACED DIRECTLY AT THE POINT OF LOAD, PERHAPS EVEN SOLDERED DIRECTLY TO THE PARALLAX SD CARD ADAPTER BOARD DEPENDING ON THE DESIGN.  
 THE VIDEO OUTPUT DAC AT R3 - R5 ASSUMES A STANDARD 75 OHM LOAD AND IS CALIBRATED TO GENERATE A 0-TV SIGNAL RANGE.

ALL ICs ON THIS SHEET ARE SOCKETTED.

# ANALOG INPUTS

ALL OF AMPS ARE TLV2374. SEE POWER SUPPLY SECTION FOR DECOUPLING INFORMATION.  
 ALL RESISTOR NETWORKS ARE 5% TOLERANCE.  
 ALL DIODES ARE BAT185S.

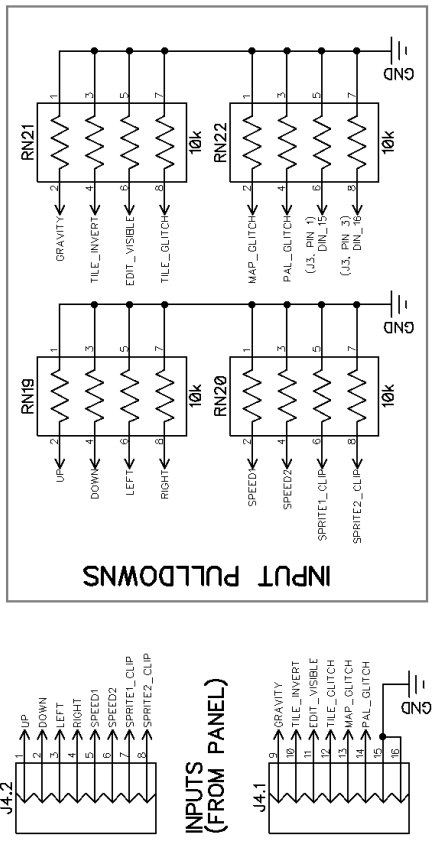
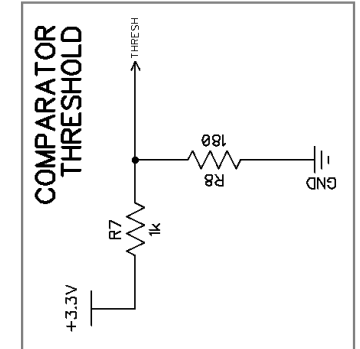
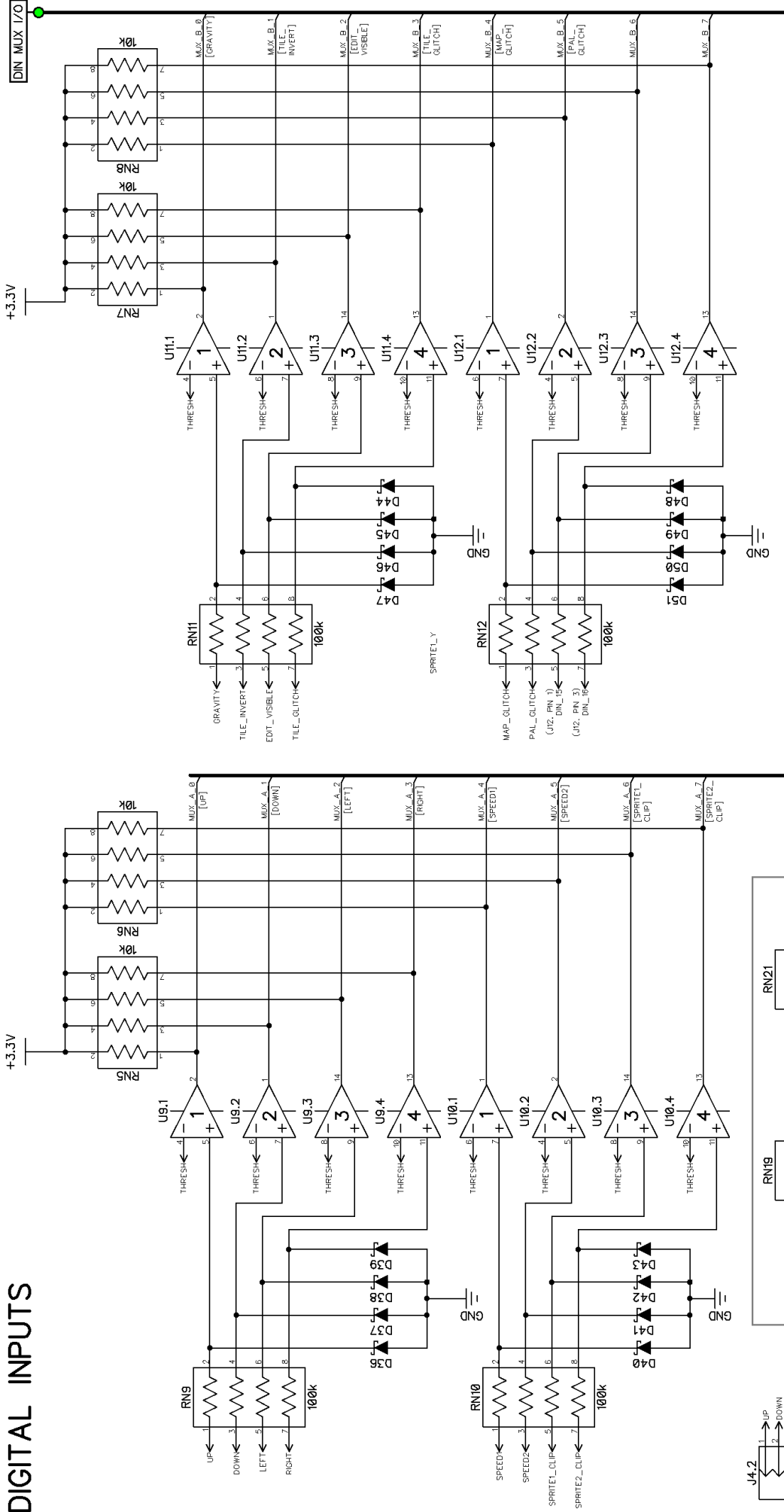
## INPUTS (FROM PANEL)



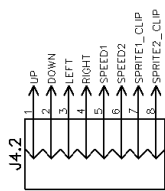
POST-BUFFER SIGNALS HAVE THEIR CORRESPONDING JS NAMES WRITTEN IN BRACKETS.  
 OVERVOLTAGE PROTECTION DIODES ARE CLAMPED TO A SEPARATELY BUFFERED 5V RAIL TO AVOID SINKING CURRENT TO THE 7805 VOLTAGE REGULATOR. SEE POWER SHEET FOR THE CLAMP RAIL CIRCUIT.

ADC I/O

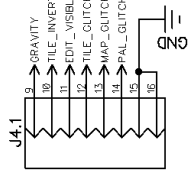
# DIGITAL INPUTS



INPUT PULLDOWN RESISTORS ARE INSERTED UPSTREAM OF 100K SERIES RESISTORS  
 ALL RESISTOR NETWORKS ARE 5% TOLERANCE.  
 POST-BUFFER SIGNALS HAVE THEIR CORRESPONDING J4 NAMES WRITTEN IN BRACKETS.  
 ALL COMPARATORS ARE LM339N. SEE POWER SHEET FOR SUPPLY AND DECOUPLING INFORMATION.  
 ALL DIODES ARE BAT85S.  
 COMPARATOR THRESHOLDS ARE HELD AT 0.5V AS SET BY THE R7/R8 VOLTAGE DIVIDER.  
 R7 AND R8 ARE 1% TOLERANCE OR BETTER.  
 R26 AND R27 ARE 5% TOLERANCE.



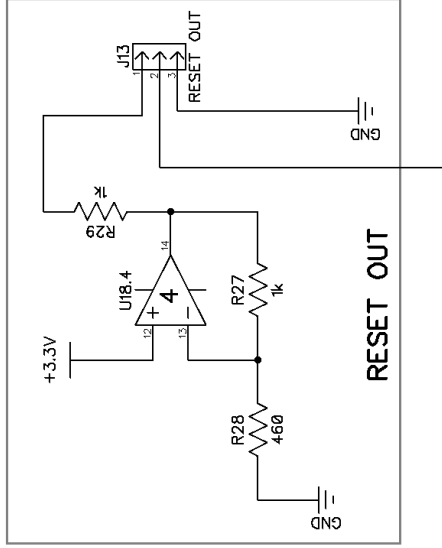
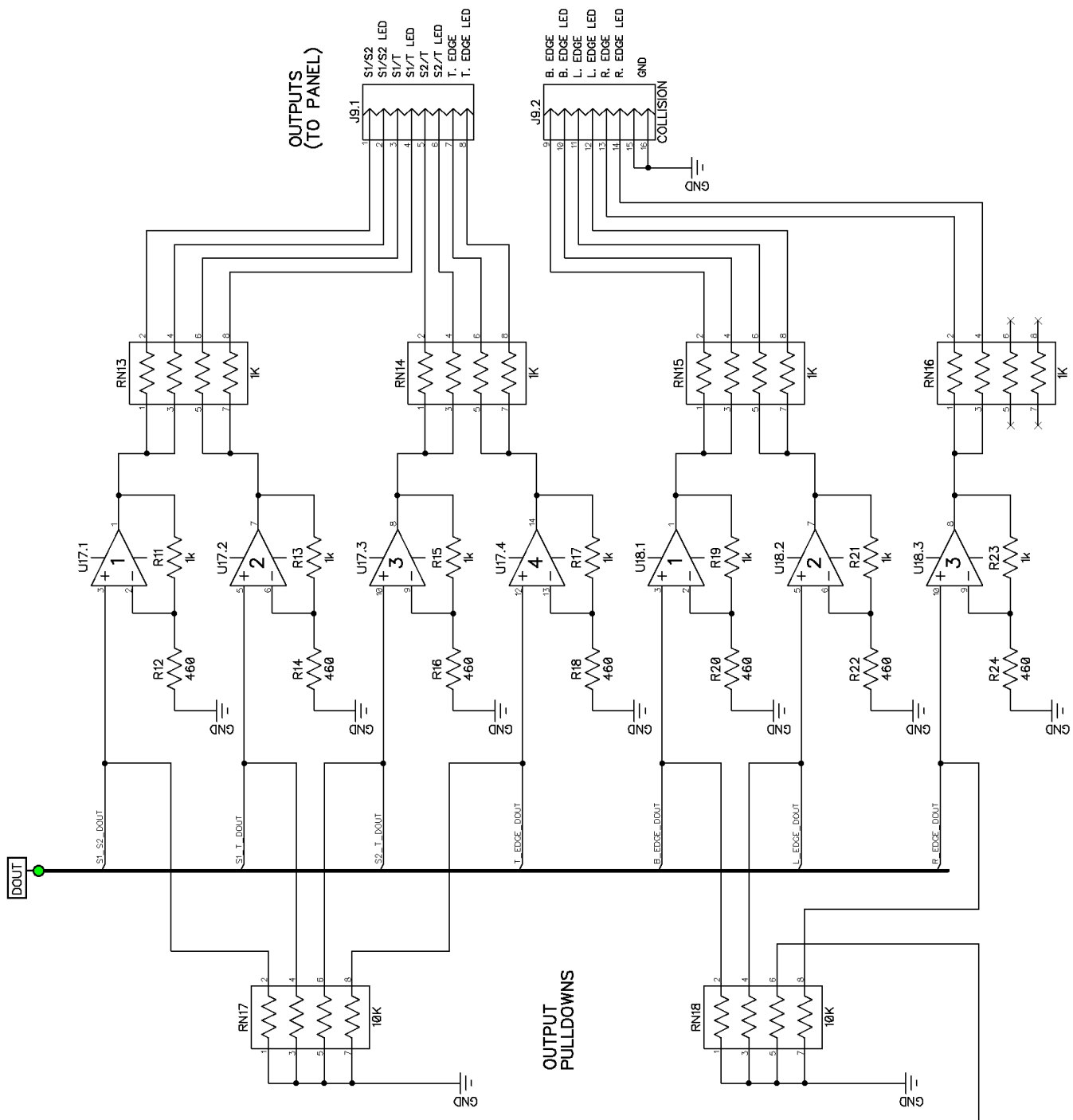
**INPUTS (FROM PANEL)**



# DIGITAL OUTPUTS

ALL RESISTOR NETWORKS ARE 5% TOLERANCE.  
 R11 - R24, R7, AND R28 ARE 1% TOLERANCE OR BETTER.  
 OP AMP GAIN IS CALIBRATED FOR 10.5V GATE OUTPUTS.

NOTE:  
 THE "RESET\_OUT" CIRCUIT BLOCK HAS DIFFERENT OUTPUT WIRING THAN THE COLLISION OUTPUTS AT J9. J13, PIN 1, CONNECTS TO A MOMENTARY TOGGLE, AND THE PULLDOWN RESISTOR AT J13, PIN 2, CONNECTS TO THE OUTPUT JACK POST TOGGLE. SEE PANEL WIRING SHEET FOR MORE INFORMATION.



## RESET\_OUT

## OUTPUT PULLDOWNS

## OUTPUTS (TO PANEL)