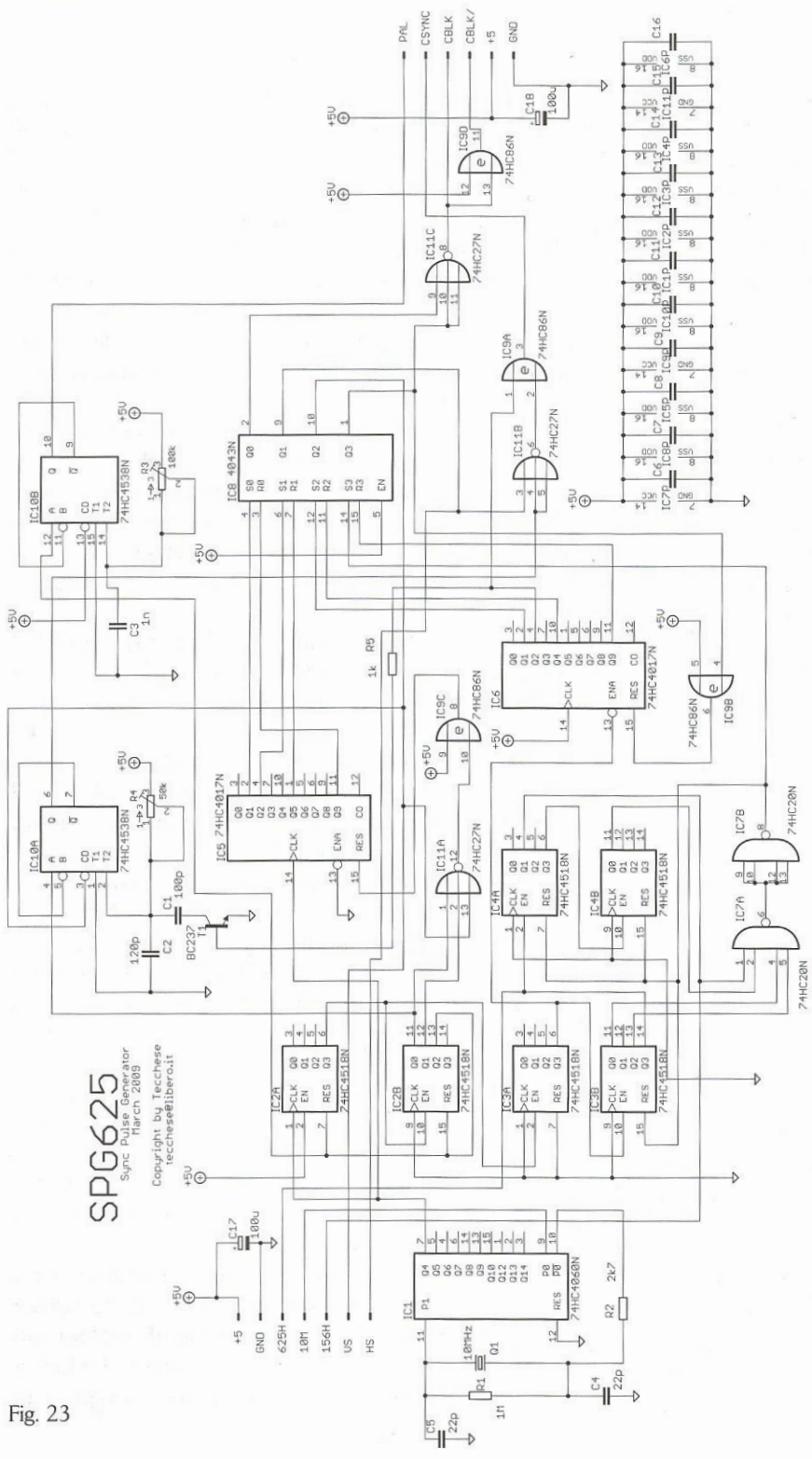
SPG625
Sync Pulse Generator
March 2009
Copyright by Tecchese
tecchese@libero.it
PAL
CSYNC
CBLK
CBLK/
+5
GND
625H
10H
156H
VS
HS
74HC4538N
74HC4017N
74HC4518N
74HC4060N
74HC86N
74HC27N
74HC20N
4043N
BC237
10MHz
1k
2k7
1M
22p
120p
100p
50k
100k
100u
1n

Fig. 23

plication of both ICs for PAL-ready CCIR625 system.

In January 1990 Philips introduced the SAA1101, considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC. This device is now discontinued but it is still available from *Donberg Electronics LTD* (www.donberg.ie) or *Littlediode* (www.littlediode.com). For knowing its improved features, you can cast a glance to its datasheets still available on Philips's website.

The German Siemens also designed a SPG chip, the *S178A*, a MOS digital component which generated all the pulses necessary in a television through internal dividers, starting from a high clock frequency. You could also program all the numbers of lines up to about 1500, as well as six different sync waveforms. 10-bit binary line number codification inputs are available for odd numbers of rows (interlaced system), or for even numbers of rows by translating the numbers of those lines you want to see in its equivalent binary number. With inputs N_A, N_B and N_C, the functions dependent on standards, such as number of equalization pulses, are adjustable. It was distributed in a 28 pin DIL package and in Fig. 21 there is its block diagram. It is still distributed by Littlediode but it is quite expensive.

Even Sony made some SPG chips, most of them designed for broadcast video cameras as the *CXD1159AQ, CXD1217M, CXD1254AR, CXD1257AR, CXD1261AR*. In Fig. 22 there are the block diagram and pin configuration for CXD1217M.

Other industries made single chip SPGs as Hitachi (*HD44007A*), Panasonic (*MN67603NS* and *MN67621P*) and NPC (*SC6433* - NTSC only).

When technology made it possible to create a simple, full broadcast, multi standard SPG with a single PIC microcontroller suitably programmed (also capable of generating computer video frequencies and patterns), the production of the SPG chips was slowly stopped.

Currently in production there remains only Fairchild's *74ACT715* (available from Farnell), described as a *Programmable Video Sync Generator* and equivalent to the discontinued National's *LM1882*.

This is a wholly programmable device which can produce almost any set of video timing waveforms. It is designed to give NTSC 525 line waveforms by default but other line system waveforms can be generated. It requires some ingenuity to achieve this because registers need to be loaded with the correct numbers every time it is switched on and Fairchild does not generally reveal any application notes for performing this operation.

The 74ACT715 datasheet can be easily downloadable from Fairchild website (www.fairchildsemi.com).

2.4.2 Multiple chip SPGs.

Until now we talked only about single chip sync generators, but is there a possible means to design a CCIR625 compliant generator using only standard ICs?

The answer is affirmative and in Fig. 23 there is an example of diagram. I named this circuit **SPG625**.

This equipment should preferably be constructed by those with some experience of digital circuits and own an oscilloscope, because the circuit is quite complicated.

This unit has been built using 'only' eleven standard CMOS ICs. Thanks to their exclusive use, the power required by this SPG is low and therefore highly suitable for other video applications for which low overall consumption instruments are required.

Unlike most simple solutions based on ordinary ICs, this circuit also generates pre & post equalization pulses, broad pulses, composite blanking signal, switching PAL pulse and interlaced fields, as well as composite vertical and horizontal sync pulses starting from a unique master clock.

All waveforms are obtained by a train of pulses 1.6µs wide derived by dividing the 10 MHz crystal oscillator by 16 through the oscillator/divider IC1 (74HC4060). The 1.6µs pulses leave Q4 of IC1 and are applied to the inputs of clock of IC2A (74HC4518) and IC5 (74HC4017).

IC2 is a dual divide-by-10 counter, connected in such a way that once it reaches the number '40', both counters are cleared and counting reverts from zero.

The triple-input NOR IC11A (one of the three included in 74HC27) followed by exclusive OR IC9C (one of the four included in 74HC86), configured as an inverter, enables counter IC5 only when the IC2 is counting between 0 and 9, that is when the outputs of Q0 and Q1 of IC2B and a pulse coming from IC8/pin10 (see later about this last pulse) are at '0' logic level. Since a complete counting cycle of IC2 is 40*1.6µs=64 µs, you can obtain, according to the outputs of IC5, the horizontal signals HS and HBLK in this way: the next 1.6µS pulse sets the output Q1 of IC5 to logic state '1'; another pulse brings Q2 to the same level, and the cycle continues until IC2B reaches the number '10' and Q0 reverts to '1' and remains in this state. Then the outputs Q1 and Q9 of IC5 will drive the S0 and R0 inputs of one of the four NOR S/R Flip-Flop included in IC8 (4043) so from its output Q0 you get HBLK whose length can be calculated by measuring the timing from the two rising edge pulses coming from Q1 and Q9 of IC5, i.e. 1.6*8=12.8 µs. The 0.8 µs over the 12 µs blank timing specified in CCIR625 standard will not be critical in most cases. Similarly the Horizontal Sync is obtained from Q1 of IC8 by setting and resetting another of the four NOR S/R Flip-Flop included in IC8 through the outputs Q2 and Q5 of IC5, thus creating a pulse of 1.6*3=4.8µs. This HS pulse is delayed inside HBLK by 1.6µs, so it will be put inside horizontal blanking at the right place.

From Q3 of IC2A the pulses of width 1.6*10=16µs are then applied to IC3A (74HC4518). Since IC3A is a decimal divider, the pulses that appear on Q3 of IC3A have an interval of 160µs and are sent as clock pulses to IC6 (74HC4017) and IC3B. The decimal counters IC3B and IC4 (74HC4518) are linked together through the AND gate IC7 (74HC20): in this way, once the counter reaches the number '125', the counters IC3B, IC4A and IC4B are cleared. The counting cycle therefore will be 125x160µs=20ms: this interval matches the length of a field. To perform this operation perfectly, it is better to match IC3 & IC4 using the same brand and even production stepping if possible. The reset pulse coming from IC7B sets the S3 input of the third NOR S/R Flip-Flop included in IC8 whose output Q3 will feed IC9B (used as inverter) so that the counter IC6 is left free to work after the end of the reset signal pulse coming from IC7B.

The counter IC6, driven by a 160µS pulse train coming from Q3 of IC3A, after 8x160µs=1.28ms, reaches the state where Q9 is '1' and therefore the NOR S/R Flip-Flop will be reset via R3 input. Only a new reset of the counters IC3B, IC4A and IC4B will switch the flip-flop again. The signal from 1.28ms, and taken from the S/R flip-flop, will then be used as Vertical Blank which corresponds to 20 lines. The missing 5 lines needed for matching the CCIR625 standard are irrelevant for our final result.

The Q2 output of the last NOR S/R Flip-Flop included in IC8, through the outputs Q1 and Q4 of IC6, provides a 3x160µs=480µs pulse (corresponding to a vertical interval timing of 7.5 lines) which gates the monostable IC10A (74HC4538) and will reset IC5 through IC11A & IC9C.

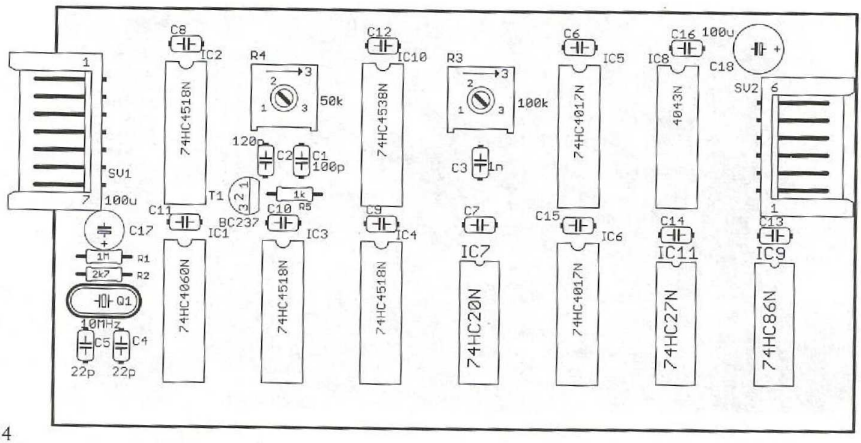

Fig. 24

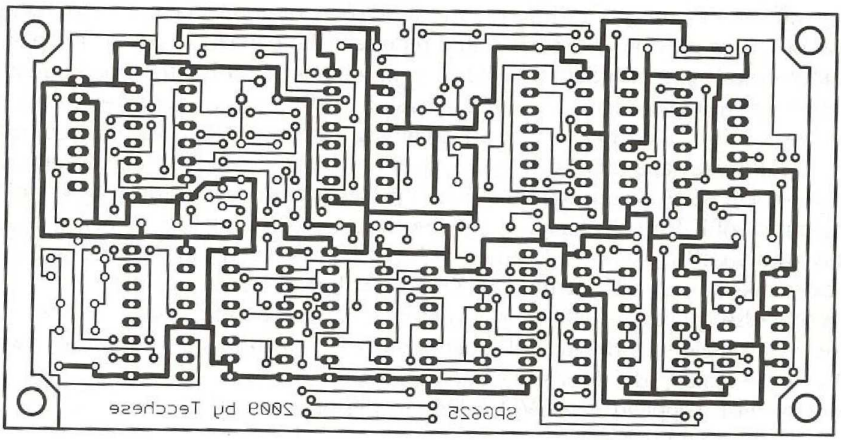

Fig. 25

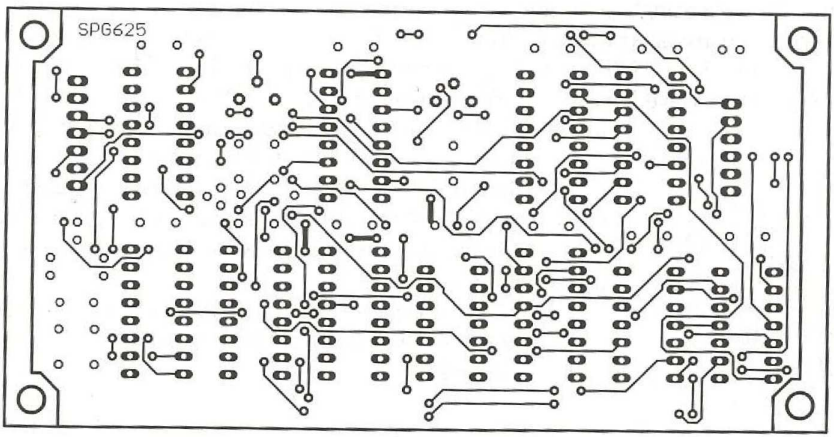

Fig. 26

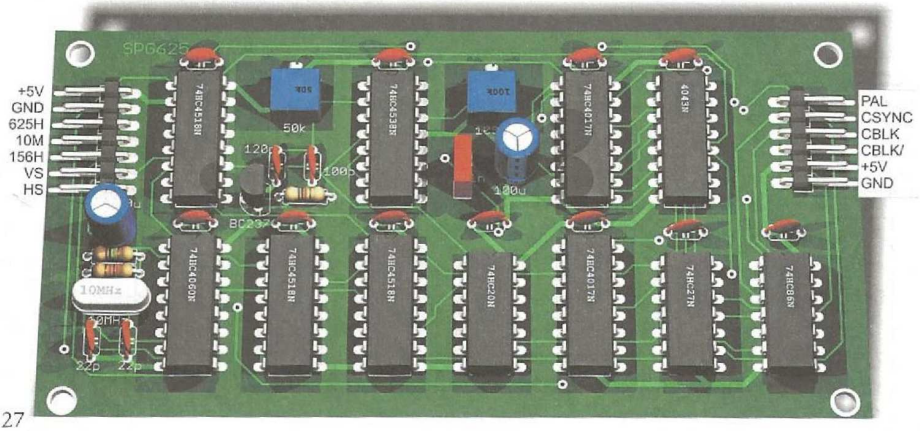

Fig. 27

The monostable IC10A is fed by pulses from Q0 of IC2B producing a pulse of 2.35µs every 32µs via R4/C2 timing. These pulses appear in place of horizontal sync during the vertical interval of 480µs previously described and represent the equalizing pulses. To enlarge the pulses inside vertical sync, in order to create the right duration of 4.7µs for broad pulses, C1 is inserted dynamically in parallel to C2 via the transistor T1 (BC547) used as an electronic switch driven only by the 160µS 'central' vertical pulse coming from Q2 of IC6 and buffered by IC9D.

NOR IC11B mixes and inverts the polarity of horizontal, broad and equalization pulses, while exclusive OR IC9A inverts again the broad pulses only since it is driven by Q2 of IC6.

At the output of IC9A will finally emerge the correct CSYNC signal with negative polarity, compatible with CCIR625 standard. Similarly, NOR IC11A inverts and mixes the horizontal and vertical blanking, thus creating the CBLK signal with its negative polarity.

The reset pulse applied to IC2, which appears at the end of a line, is drawn and used for driving the monostable IC10B, which through R3/C3 timing creates a square wave two lines wide (PAL switch signal), useful for some applications.

All the circuit is supplied by +5VDC. Due to the presence of several HCMOS IC, it is preferable not to exceed that voltage.

I designed a small single sided PCB; the top layer has a few small bridges which can be realized using some insulated wires. All the ICs should be put on sockets if simplicity is the rule.

An oscilloscope is needed in order to calibrate the SPG625. The R3 trimmer will be adjusted until a square wave is visible on the oscilloscope screen whose positive cycle must be wider than 1µS of standard horizontal timing, i.e. 65µS (probe on pin 10 of IC10B), whilst R4 trimmer is adjusted until to obtain a series of narrow pulses 2.35µS wide for 480µS (probe on pin 6 of IC10A), except during the 160µS vertical pulse where the same pulses must be 4.7µS wide.

The Fig. 24, 25 & 26 describe the main PCB layouts while in the Fig. 27 is represented a 3D picture of the SPG625.

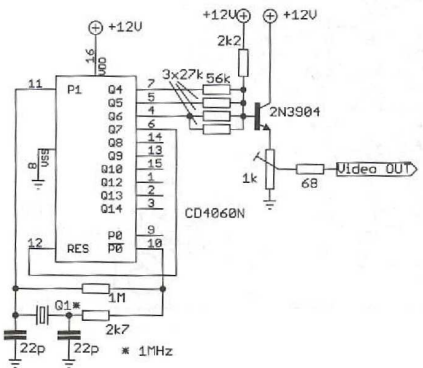

Fig. 28